Q.P. Code: 16EC5702 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester (R16) Regular Examinations December 2016

ANALOG IC DESIGN

(VLSI)

(For Students admitted in 2016 only)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

Q.1	a.	Draw the MOS transistor characteristics for enhancement mode and depletion mode.	7M
	b.	What are the deficiencies of MOS technology? How they can it be overcome.	5M
		OR	
Q.2	a.	Explain the effect of threshold voltage on MOSFET current equations.	7M
	b.	Explain briefly large signal modeling for BJT with basic current mirrors.	5M

UNIT-II

Q.3	a.	Discuss the various short channel effects in MOS devices.	5M
	b.	Draw the noise model of a source follower with necessary equations	7M
		OR	
Q.4	a.	Explain in detail about current feedback OP-amplifier..	7M
	b.	Explain latched comparators..	5M

UNIT-III

Q.5	a.	Explain MOS sample and hold circuit	7M
	b.	What is the need for double sampling techniques.	5M
		OR	
Q.6	a.	Discuss the different performance characteristics of sample/hold circuits.	7M
	b.	Explain about Switched capacitor gain circuit..	5M

UNIT-IV

Q.7	a.	Draw the schematic of 4 bit resistor based binary weighted D/A converter and explain it operation. What are the advantages of binary weighted converters?	5M
	b.	Explain the design procedure for integrates A/D converters.	7M
		OR	
Q.8	a.	Explain about interpolating A/D converters.	7M
	b.	Explain about Time interleaved A/D converters.	5M

UNIT-V

Q.9	a.	Write about Digital decimation filter.	7M
	b.	Write about over sampling without noise shaping.	5M
		OR	
Q.10	a.	Explain about practical considerations for stability..	5M
	b.	Discuss about linearity of two –level converters..	7M

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